Wideband preamp and LSI pair form high-quality counter

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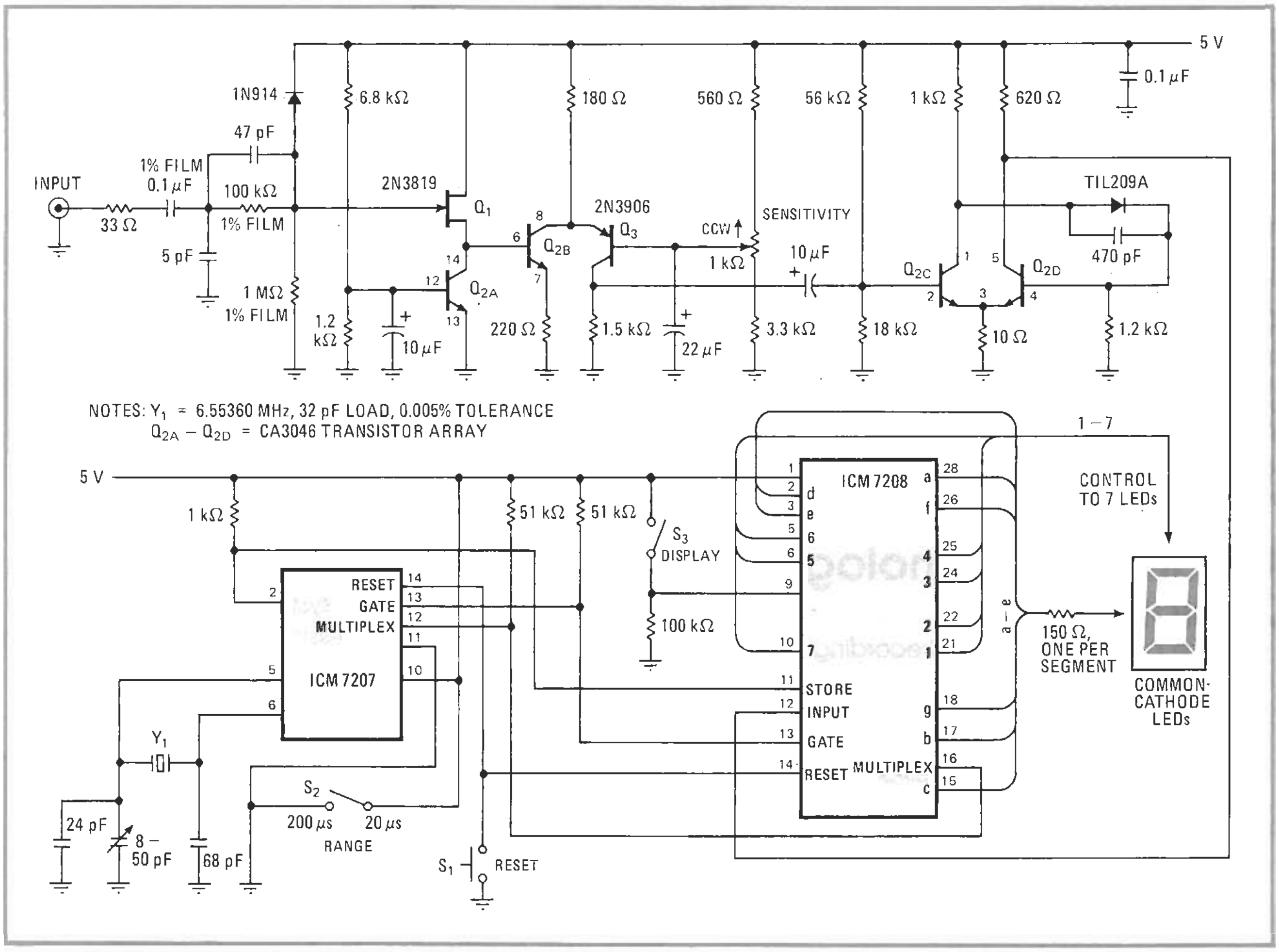
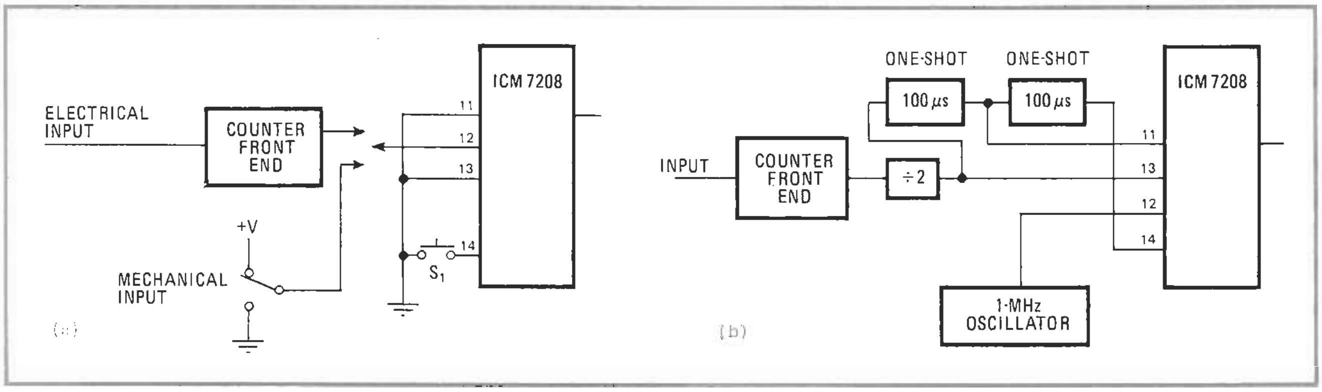
A carefully designed preamplifier, when combined with two new large-scale-integrated circuits, forms a high-performance, low-cost frequency counter with a typical response of 5 megahertz. Among this counter's many desirable qualities are a high input impedance throughout the frequency-measuring range, a frequency response that can be extended to 30 MHz, a single voltage supply and, if the displays are powered separately, a low power drain that allows battery operation.

As the figure shows, the input signal is applied to the 2N3819 field-effect transistor through a frequency-compensated attenuator. The combination of the FET and attenuator produces an input impedance of 1 megohm from 0 to 30 MHz. The input circuit is protected from overdrive by the 1N914 diode. Q_1 is a current-biased source follower, providing high input impedance, low output impedance, and high stability even at low power-supply voltages.

The amplified signal is applied to the cascode amplifier composed of Q_{2b} and Q_3. The operating (bias) point is Q_3 is adjustable over a 1-volt range, so that the triggering voltage may be properly set even with noise present on the input signal. The signal is then introduced to the Schmitt trigger composed of Q_{2c} and Q_{2d}. The circuit has a fixed hysteresis determined by the TIL209A light-emitting diode (the LED acts as a low-voltage zener), which makes triggering precise even with slowly varying waveforms. This output signal, which will



1. Frequency counter. A well-designed front end and two LSI circuits permit realization of a high-performance, low-cost frequency counter. The counter's frequency response is 5 MHz, but can be expanded to 30 MHz. Total cost is $50, half that of competitive units.



2. Easily adaptable. A slight modification to the input circuit makes it absolutely versatile. The circuit can be configured to monitor the number of electrical or mechanical events (a) or as a period counter (b) for measuring input cycle duration or the time between events.

be counted by the Intersil ICM7208, has a duty cycle of approximately 50%.

The ICM7208 contains a seven-decade counter, a display multiplexer, a seven-segment decoder, and digit and segment drivers. Additional circuits within the 7208 serve to blank the display, reset the counter inhibit input, and switch the display on and off. The device can count to 5 MHz, and the circuit draws only 1 milliampere or so at 5 v. A companion device, the ICM7207, supplies a crystal-controlled time base and other signals for multiplexing the display and controlling the sampling interval of the 7208.

The output frequency of the crystal-controlled oscillator is reduced to 1.6 kilohertz by the 7207 in order to multiplex the seven-segment LED display. The 7207 is also configured to produced a gate signal of 20 or 200 microseconds for the 7208 counter. This count window is switch-selectable. Leading-zero blanking and an on/off switch for the display are provided for energy conservation.

The circuit may be simply reconfigured as a period of event counter, as shown in Fig. 2. Additional divider stages at the counter's input and control-signal channels may be used to expand the range of the counter to 30 MHz.

This counter compares favorably with other designs. Its sensitivity at 0.1 MHz is 50 millivolts, decreasing to 200 mv at 30 MHz. The current drain is 21 milliamperes at 5 v, neglecting the LED displays. Total cost for this circuit is less than $50; a transistor-transistor-logic frequency counter would cost twice as much and might dissipate as much as 40 times the power. Commercially available units cost $200 to $300. □

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